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Modeling and Analysis of Reliability Challenges in Nanoscale Transistors

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Abstract

To meet the speed, complexity, circuit density, power consumption, and ultimately cost requirements of many advanced applications, scientists have spent decades shrinking device feature sizes for better performance of metal-oxide semiconductor (MOS) technology. However, there are several disadvantages to switching to these nano size MOS devices. Most of the functional failure in nano-scale devices is caused by aging related phenomena such as negative bias temperature instability (NBTI), hot carrier degradation (HCD), and time dependent dielectric breakdown (TDDB). However, Silicon devices' dimensions and material capabilities are beginning to hit their limitations. Scientists and researchers have figured out how to replace the current silicon material with an emerging novel material like carbon nano tube. The goal of this research was to develop a drain current and threshold voltage model for carbon nanotube field effect transistors (CNTFETs) that can be used in the analysis and design of reliable integrated circuits, focusing on the reliability issues of conventional metal oxide semiconductor field-effect transistors (MOSFETs) at the nanoscale. To develop this model, we investigated the atomic structure of carbon nanotubes and used the fundamentals of electrostatics to describe a field-effect transistor. By analyzing and defining the electronic structure of carbon nanotubes, we first arrived at analytical formulas for the carrier concentration in carbon nanotubes for various chiral vectors (n, m). By combining several chiral vectors, it is possible to determine the threshold voltage expression that is obtained throughout the procedure as well as the I-V characteristics for CNTFETs. The diameter and chiral angle of carbon nanotubes were shown to be significant determinants of the I-V characteristics and threshold voltage. In terms of the threshold voltage change CNTFET shows better performance 24% less than the conventional MOSFET in 45nm technology node.

Keywords: MOSFET; Negative Bias Temperature Instability; Hot Carrier Degradation; Time Dependent Dielectric Breakdown; Carbon Nanotube; Chiral Vector; Threshold Voltage.

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1. INTRODUCTION

The reduction in the size of MOSFETs is driven by the need for increased circuit speeds and higher packing densities. For over six decades, Moore's law has been the driving force behind technological advancement and innovation in the semiconductor industry [1]. It predicts a doubling in the number of transistors approximately every two years [2]. It survived as a self-fulfilling prophecy. Many engineering fields require balancing performance, power, and cost. As transistor size decreases, their speed, power dissipation, and manufacturing cost also decrease [3]. As a result of this convergence, not only have electronics been transformed, but also environment impact at a large.

A failure occurs when the system is not operating according to its specifications for an extended length of time. Faults, which are defined as the failure of a subsystem, are the root cause of all failures. There are several potential origins of malfunctions, including mistakes in the design phase, flaws in the manufacturing process, normal wear and tear, environmental factors, and even malicious usage. While certain flaws are bound to lead to mistakes, others might go undetected. For instance, a single-processor system is immune to errors brought on by flaws in the multiprocessor interface logic. If a bad via is next to a good one, nobody may know it is there. The failure rate of the system may be predicted and improved by studying the underlying defects. The threshold voltage and gate leakage both change when the gate oxide degradation from repeated stress. When the transistors are too old, the mismatches get too big, and the leakage current is too high, and the consequences are

circuit breaks down [4]. To reduce the negative impacts of oxide, wear out during a MOSFET lifespan, most processes set a maximum operating voltage [5]. Negative Bias Temperature Instability (NBTI), Hot Carrier Degradation (HCD) and Time Dependent Dielectric Breakdown (TDDB) are the three main reliability issues that causes due to oxide degradation.

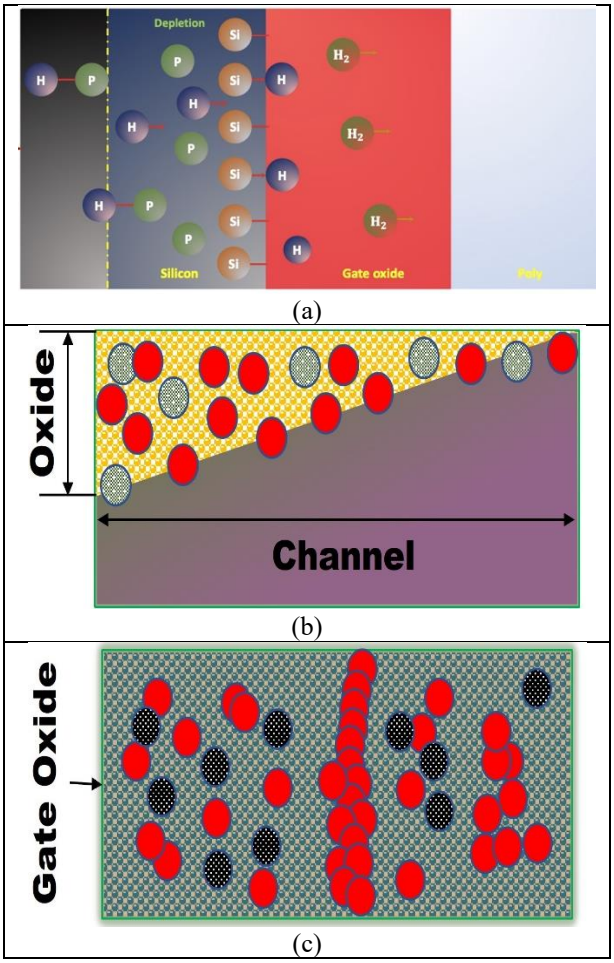


Figure 1: Principle of three main reliability issues: (a) NBTI, (b) HCD and (c) TDDB. The increase in operation time is associated with these reliability issues

These reliability issues are the big concern in nanoscale domain especially for silicon based MOSFET technology showing in Figure 1 [4-6]. Besides, silicon devices are reaching the limits of dimension and material scaling. Therefore, the IC industry is anticipating that silicon devices will be unable to meet the demands of nanoscale technology. The International Technology Roadmap for Semiconductors (ITRS) believes that silicon will reach its dead-end by decade [2]. Scientists and researchers have been exploring emerging materials like carbon nanotube (CNT) based nanotechnology to replace silicon technology. Due to the ultra-high carrier mobility and quasi-ballistic transport, CNT has been considered as a promising channel material for constructing the future FETs. Introducing CNT based transistor could be a potential solution to resolve the reliability issues that occur in current semiconductor technology [7].

Therefore, this study examines the reliability of MOSFETs and the challenges arising from technology scaling. Additionally, a novel material is proposed as a potential replacement of silicon i.e., carbon nanotube. Reliability improvement usually implies performance loss. The tradeoff between speed and reliability must be made when deciding on a device architecture for use in scaling technologies. Now that large reliability margins can no longer be afforded, it is more crucial than ever to use enhanced knowledge, more precise modeling, and more thorough analysis to ensure that the necessary device reliability exists under field-operation conditions while enabling the maximum possible device performance.

2. MATERIALS AND METHODS

2.1. Background of Carbon Nanotube Field Effect Transistor (CNTFETs)

The dimensions on the scale of the quantum mechanical wavelength of electrons are possible to produce in carbon nanotube field effect transistors (CNTFETs). Therefore, quantum mechanical considerations and ballistic transport affect the transport

parameters [8, 9]. Figure 2 illustrates the fundamental cylindrical configuration of a CNTFET, n-type and p-type compact model of CNTFET. Laboratory fabrication of both n-type and p-type CNTFETs has occurred since CNTs may dope with n-type and p-type impurities. The CNTFET structure resembles that of a conventional MOSFET, with a single-walled carbon nanotube (SWCNT) serving as the channel between two electrodes functioning as the source and drain of the transistor [10, 11]. The structure is constructed on top of a silicon substrate serving as the back gate and an insulating layer [12]. The manufacture of CNTFETs has shown substantial development during the last two decades [13]. There are a wide variety of devices that use CNTFETs, such as n- and p-type CNTFETs, multistage complementary logic gates, CNT-interconnections, and SRAM cells. The following are the procedures required to create a CNTFET: One may determine the diameter of carbon nanotubes generated by any of the techniques [14]. Alignment markers for the carbon nanotube's metal electrodes are based on the location of the catalyst pattern. The source and drain contacts are these metal electrodes. The Schottky barriers at the drain and source contacts may be eliminated or reduced when using palladium (Pd) or calcium (Ca) electrodes [15]. Gold (Au) and titanium (Ti) electrodes have also been employed. The gate contacts and gate oxide, which are typically silicon nitride and have a high k-dielectric constant [16], are provided. The gate capacitance and gate coupling of the device have been improved [17] by using high k-dielectric materials. The successful fabrication of both n-type and p-type CNTFETs has been previously mentioned. The initial fabrication of CNTFETs demonstrated p-type behavior in their I-V characteristics, suggesting the presence of p-type doped carbon nanotubes. The p-type behavior can be attributed to the absorption of oxygen, as demonstrated in studies [18]. This absorption alters the energy band level diagram at the interface between the carbon nanotube (CNT) and the electrode, promoting the conduction of holes. The n-type carbon nanotube field-effect transistors (CNTFETs) were fabricated in previous studies [19]. Derycke *et al.,*[20] demonstrated the fabrication of n-type CNTFETs through vacuum annealing for a few minutes. Conventional doping has been used to fabricate n- and p-type carbon nanotube field-effect transistors (CNTFETs). Potassium (K) has been used to create n-type devices as a donor agent, while boron (B) has been used to create p-type devices.

2.2 Proposed CNT Based Device Structure

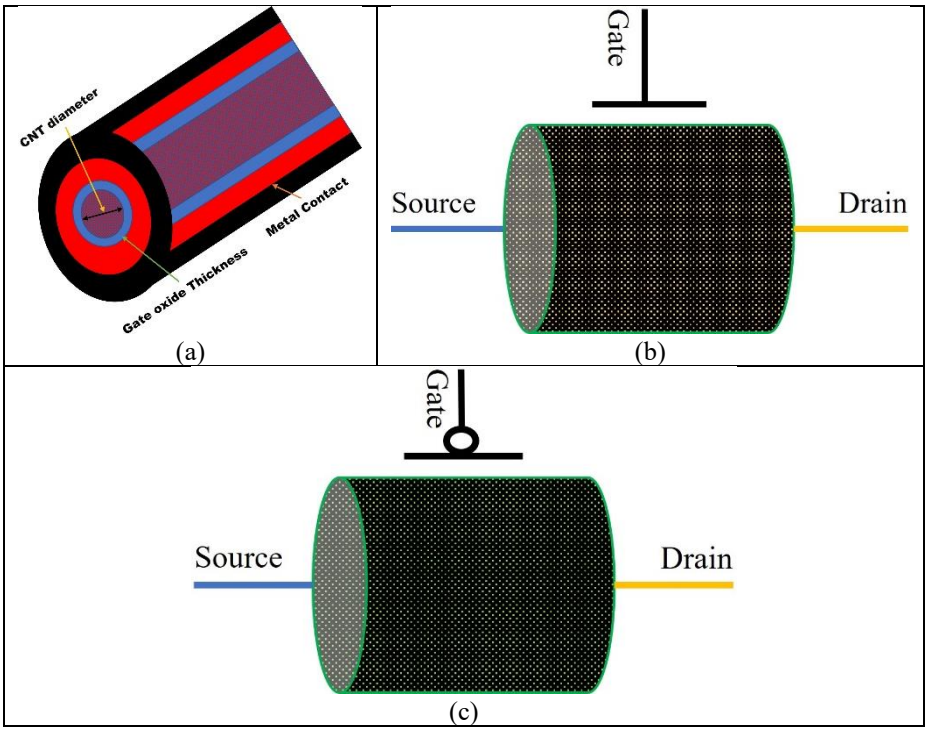


Figure 2: Fundamental structure of Carbon Nanotube based Transistor: (a) Cylindrical structure of CNTFET, (b) n-type compact structure and (c) p-type compact structure

For future nanoelectronics, CNT is a possible alternative to current silicon technology due to its distinct electrical characteristics. Allotropes of carbon are what CNTs are modified to be. Instead of using bulk silicon as in a conventional metal-oxide-semiconductor field-effect transistor (MOSFET), a single CNT is used as the channel material in a carbon nanotube field-effect transistor (CNTFET). When compared to other materials, particularly silicon, CNTs stand out for their superior stiffness, strength, and firmness [21-22]. The sheets of graphene that make up carbon- nanotubes are seen coiled up. Graphene has the potential to be the strongest material ever tested but extracting it from graphite will need significant improvements in

technology before it can be utilized economically in industrial operations. CNT is characterized by a flawless crystalline structure made up of strong covalent C-C bonds where nanotubes are seen coiled up. Graphene has the potential to be the strongest material ever tested but extracting it from graphite will need significant improvements in technology before it can be utilized economically in industrial operations. CNT is characterized by a flawless crystalline structure made up of strong covalent C-C bonds. The ability of carbon to build lengthy chains of its own atoms, known as catenation, makes it unique among all other elements. When compared to competing semiconductor devices built using standard silicon technology, SWCNTs are seen as a potential contender.

The structure of a carbon nanotube field-effect transistor (CNTFET) closely resembles that of a silicon metal-oxide-semiconductor field-effect transistor (MOSFET), with the exception that a carbon nanotube is incorporated into the transistor and serves as the channel. The CNTFET functions similarly to the MOSFET, with electron movement occurring between the source and drain terminals. The simulation focuses on a CNTFET model with a single walled carbon-nanotube, an intrinsic channel region, and a chirality of (7,2). Gold and Palladium are commonly used as external source/drain contacts in CNTFET. Assuming metallic contacts, the work function differences between the source contact (7,2) and the CNT, as well as between the drain contact and the CNT, and the gate contact and the CNT, are all assumed to be 0.41 eV.

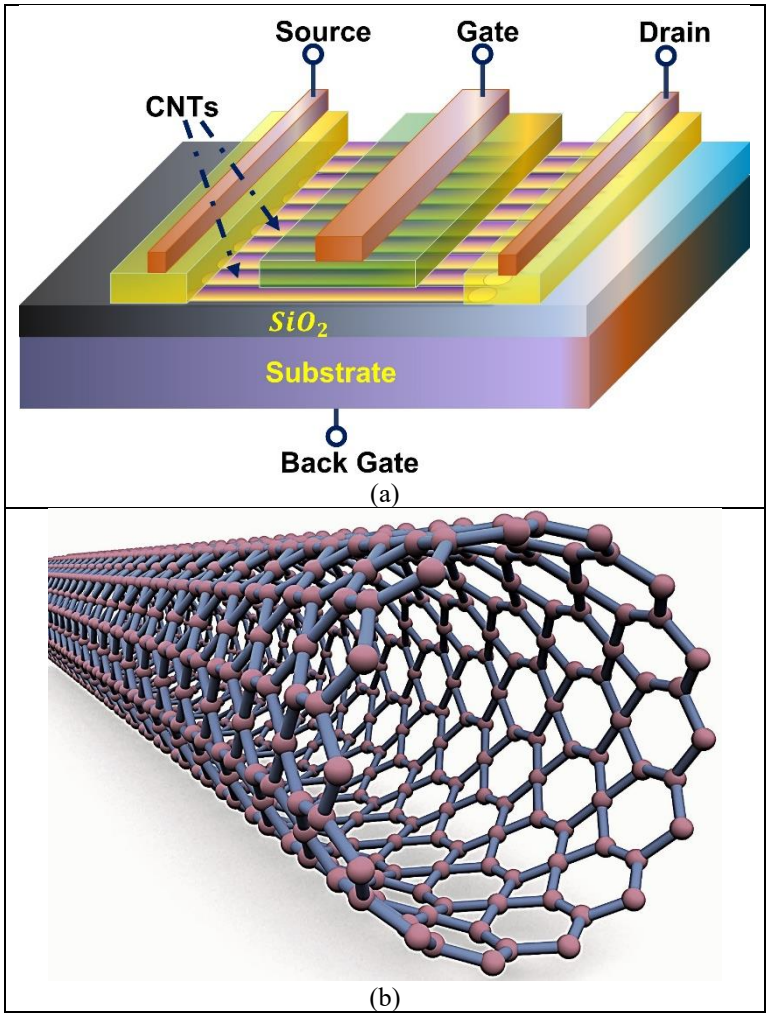


Figure 3: Proposed Device Structure of CNTFET where SWCNT use as channel material

Figure 3 represents the proposed device structure where SWCNT is shown as the channel material in a CNTFET schematic. The device structure has a channel length of 45 nm. All the channel's essential features, as well as the source and drain extensions, are under 15 nm in width. There is a 1 nm diameter (d_{cnt} = 1 nm) chirality (7, 2) single walled carbon nanotube sandwiched between two 2 nm thick (tox) layers of HfO_2, whose relative dielectric constant is 25. The source and drain extension regions utilize a dopant density of N_{SD} =1×10^9 m^{-1}, while the channel beneath the gate contact remains undoped. The CNTFETs utilize HfO_2 for most of their structure, with SiO_2 for the channel and a drain region dielectric thickness of 3 nm (relative dielectric constant r = 3.9). The proposed structure utilizes a uniform impurity concentration of N_{SD} =1×10^9 m^{-1}

throughout the channel, extending from the source to the drain. Additionally, two isolated gates are employed to emulate the behavior of a tunnel field-effect transistor. To provide isolation between the top gate (TG) and the back gate (BG), a 3 nm long SiO_2 layer is employed. The main gate is the transistor's control gate, and its voltage may be adjusted as needed. However, the P-gate, which causes the CNTFET's source to operate like a P^+ region, has a set optimal value of 0.8 V and a fixed optimum length of 12 nm. The tight binding approximation parameters t and a_{cc} are -2.7 eV and 1.42 Å, respectively.

2.3 Drain Current Model

The current in CNTFETs is provided by [23, 24], and it is produced by both diffusion and drift carrier transport processes.

$$I_d = I_{diff} + I_{drifft} \tag{1}$$

$$I_d = \frac{|R|L}{2}\left[\int_{\varphi_{cnt,z}(0)}^{\varphi_{cnt,z}(L)} \mu(-Q_{cnt})d\varphi_{cnt} + \frac{kT}{q}\int_{Q_{cnt}(0)}^{Q_{cnt}(L)} \mu\, dQ_{cnt}\right] \tag{2}$$

In equation (2), R represents the circumference of the nanotube, while μ represents the carrier mobility within a carbon nanotube. The charge per unit area is utilized to demonstrate the inclusion of a surface area of $\frac{|R|L}{2}$ for the carbon nanotube. The mobility of each carbon nanotube (n, m) can be represented as $\mu = \gamma\mu_{graphite}$, where γ is a conversion factor that ranges from 0 to 1, accounting for the varying mobility values of different CNTs compared to graphite. Furthermore, γ can be employed to indicate the extent of the CNT's surface area that contributes to the flow of charge. The charge, $Q_{cnt,}$ can be determined in the following manner in equation 3 to 7:

$$Q_{cnt} = C_{ox1}\left(-V_{gb} + \varphi_{cnt,z} + V_{fb}\right) \tag{3}$$

$$\varphi_{cnt,z} = \frac{V_{gb} - \delta Ie^{-1} - V_{fb} + \delta m\left(V_{cb} - \frac{\Delta E_F}{q} + \frac{E_c}{q} - \frac{kT}{q}\right)}{1 + \delta m} \tag{4}$$

$$m = \frac{\sqrt{\frac{2E_c}{kT} + 1} - Ie^{-1}}{\frac{2kT}{q}} \tag{5}$$

$$\delta = \frac{qLN}{C_{ox1}} \tag{6}$$

$$\Delta E_F = \pm kT \ln\left(1 + \frac{N_D}{n_{cnt}}\right) \tag{7}$$

3. RESULTS AND DISCUSSION

The observed phenomenon can be attributed to quantum confinement occurring at nanometer-scale channel lengths. Figure 4 illustrates the relationship between threshold voltage and channel length for both CNTFET and MOSFET devices. The threshold voltage of a MOSFET decreases as the channel length decreases beyond 20 nm. This can result in the inability of the device to turn off, leading to increased leakage power consumption and ultimately device degradation. In addition, Figure 5 depicts the voltage – current characteristics in the logarithmic scale to find the subthreshold swing (mV/decade), ON – current, OFF – current and transistor gain for switching applications. Subthreshold swing (SS) is found 95 mV/decade with the chiral index (7,2) which is comparable with the traditional MOSFET. The utilization of CNTFET devices in the nanometer scale offers the benefit of an elevated threshold voltage, particularly for channel lengths of 10 nm and smaller. The impact of chiral vector variation on the threshold voltage in carbon nanotube field-effect transistor (CNTFET) devices is analyzed. These findings indicate that a lower chiral vector value corresponds to a higher threshold voltage, while a higher chiral vector value corresponds to a smaller threshold voltage. The analysis of the impact of channel length on the threshold voltage of CNTFET and MOSFET devices reveals that as the channel length decreases to 10 nm or below, the threshold voltage of CNTFET increases, whereas in MOSFET, it decreases abruptly. In terms of the threshold voltage change CNTFET shows better performance 24% less than the conventional MOSFET in 45nm technology node. Theoretical findings demonstrate agreement with extrapolated threshold voltage variation, as well as a comparison with MOSFET. The CNTFET exhibited superior performance compared to the MOSFET in terms of threshold voltage variation, indicating that the CNTFET is a more reliable option than the MOSFET.

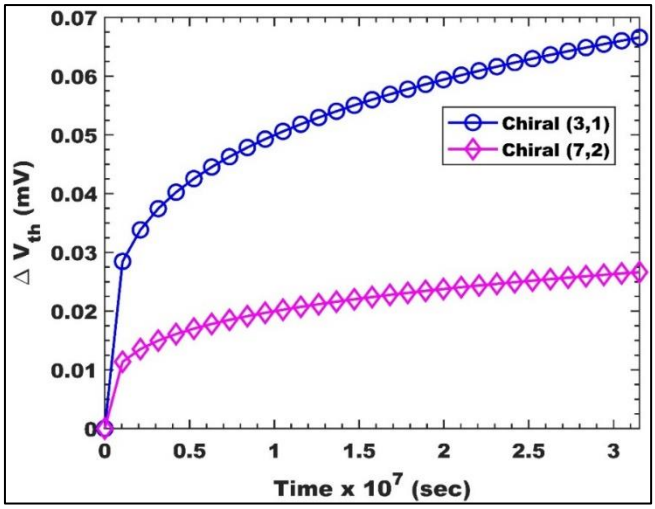


Figure 4: Change of Threshold Voltage in Proposed device over time

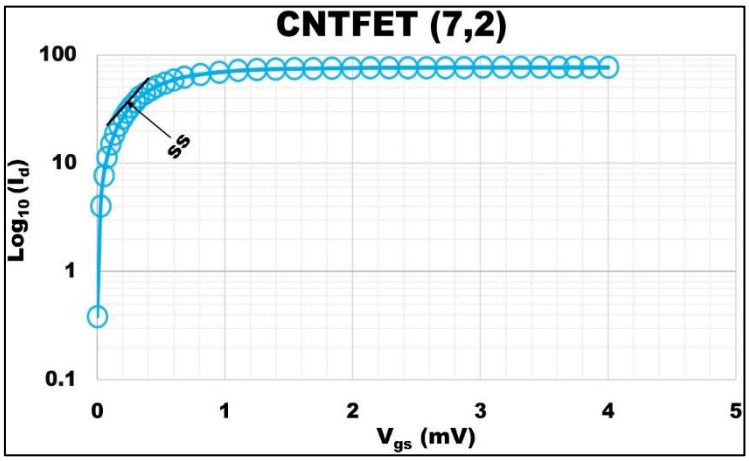


Figure 5: Subthreshold slope for proposed device

4. CONCLUSION

The dimensions and material capabilities of silicon devices are reaching their limitations because of ongoing technology scaling. Therefore, this research attempted to evaluate the performance of carbon nanotubes as a potential channel material for field-effect transistors, comparing them to silicon. Specifically, it is focused on the impact of chirality engineering. We conducted a study to analyze the physical and electrical properties of carbon nanotubes. The density of states function and band energy structure of carbon nanotubes (CNTs) were utilized to obtain an analytical solution for determining carrier concentration and effective mass in CNTs. The obtained solutions are subsequently employed to analytically characterize the current transport and threshold voltage model in a carbon nanotube field-effect transistor (CNTFET), considering the chiral vector and device geometry. The current model derived from the study was employed to generate the current-voltage (I-V) characteristics of carbon nanotube field-effect transistors (CNTFETs) with two distinct chiral vectors, namely (3,1) and (7,2), at the 45nm technology node. Additionally, it is examined the response of the threshold voltage with various parameters. The threshold voltage change of CNTFET shows better performance 24% less than the conventional MOSFET in 45nm technology node. Theoretical findings demonstrate agreement with extrapolated threshold voltage variation, as well as a comparison with MOSFET. The CNTFET exhibited superior performance compared to the MOSFET in terms of threshold voltage variation, indicating that the CNTFET is a more reliable option than the MOSFET.

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